

means for programming individual electrically-erasable reference cells of the plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

12-74. A memory circuit according to claim 69 wherein the nonvolatile memory is flash electrically-erasable and programmable memory.

13-75. A circuit comprising:
an interface circuit for interfacing to a nonvolatile memory, the nonvolatile memory including an individual memory cell, the interface circuit including a comparing circuit for comparing a data level of the individual memory cell to a reference data level;

a programmable and electrically erasable reference cell circuit generating the reference data level of a plurality of reference data levels defining a plurality of data states of the individual memory cell;

a first plurality of conductive lines coupling the interface circuit to the reference cell circuit;

a second plurality of conductive lines for coupling the interface circuit to an erase voltage source; and

a plurality of switches alternatively blocking the first plurality of conductive lines while coupling the second plurality of conductive lines and coupling the first plurality of conductive lines while blocking the second plurality of conductive lines.--

REMARKS

The present application, at page 11, lines 27-31, incorporates by reference another application entitled "Multi-State EEPROM Read and Write Circuits and Techniques", filed on the same day as the initial parent to the present application, namely April 13, 1989, by Sanjay Mehrotra and Eliyahou Harari, two of the inventors who are also named in the present application. This incorporated application is Serial No. 07/337,579, now abandoned, continuations-in-part of which have issued as patents nos. 5,163,021 and 5,172,338. The present amendment inserts a majority of the incorporated Serial No. 07/337,579 into the present application.

Therefore, essentially all of the Summary of the Invention, Brief Description of the Drawings and Description of the Preferred Embodiments sections of Serial No. 07/337,579 are being added to the present application. In the course of doing so, the patent numbers for referenced

applications have also been added. A major revision that has been made to this added text is a change in the drawing figure numbers. Figures 1-17 of Serial No. 07/337,579 are being renumbered herein as figures 9-25, respectively, in order not to use any of the same figure numbers previously used in the present application. Tables 1 and 2 of the incorporated application have also been relabeled as figures 26 and 27, respectively. Further, the reference numbers of the drawings have been changed by adding 1000 to the reference numbers of the figures being incorporated from Serial No. 07,337,579, in order to avoid duplicating the reference numbers already used in the original figures of the present application. Corresponding changes have been made to the text of Serial No. 07/337,579 that is being inserted into the present application.

The claims being substituted into this application are being copied from patent no. 5,774,395 of Richart et al., granted June 30, 1998. Newly substituted claims 63-67 and 68-73, are exact copies of claims 9-13 and 15-20, respectively, claim 74 is an altered version of claim 22, and claim 75 is an exact copy of claim 1, of the Richart et al. patent.

Inventorship:

As a result of preparing the present interference request, it has been recognized that less than all the inventors named in the present application are properly named inventors of the subject matter now claimed. Accordingly, a Petition Under 37 C.F.R. 1.48(b) To Delete Named Inventor is being filed herewith to delete one of the three inventors from this application, leaving Dr. Eliyahou Harari and Sanjay Mehrotra as the named inventors.

Favorable consideration of the present continuation application is solicited.

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Respectfully submitted,

Gerald P. Parsons

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE PC
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

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